REMARKS

Applicant thanks the examiner for his time and comments during the telephone interviews held on November 30, 2006, and December 4, 2006, which were attended by Examiner Luu and applicant's undersigned attorney, Ido Rabinovitch. During the Examiner's Interviews, the claims and the cited art were discussed. The examiner indicated that the rejections of claims 1-25 made in the August 23, 2006, Office Action, will be withdrawn. As requested by the examiner, provided herewith are applicant's comments, as discussed during the telephone interviews, regarding the outstanding rejections.

Claims 1-25 are pending in the above-identified application. Claim 1 is independent.

The examiner rejected independent claim 1, as well as dependent claims 3-7 under 35 U.S.C. §102(e) as being anticipated by U.S. Publication No. 2002/0045355 to Chong et al. The examiner rejected claims 8-12 under 35 U.S.C. §103(a) as being unpatentable over Chong in view of U.S. Publication No. 2002/0076936 to Iguchi, and rejected claims 2 and 14-25 under 35 U.S.C. §103(a) as being unpatentable over Chong in view of U.S. Patent No. 6,335,218 to Ota and further in view of U.S. Patent No. 6,008,539 to Shibata.

With respect to applicant's independent claim 1, the examiner stated:

> Chong discloses a method for manufacturing a semiconductor device with
> (1) providing a semiconductor body containing a substrate (120) and at least one nitride compound semiconductor disposed (122) on the substrate (120) (see Figure 6);
> applying a metal layer to a surface of the semiconductor body (see Figure 22);
> dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal layer (see paragraphs [0067]-[0068], Figures 6-8); (Office Action, pages 2-3)

Applicant respectfully disagrees with the examiner's characterization of Chong.

Applicant's independent claim 1 recites "providing a semiconductor body containing a substrate and at least one nitride compound semiconductor disposed on the substrate; applying a metal layer to a surface of the semiconductor body; and dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal

layer." Thus, applicant's independent claim 1 requires that at least one "nitride compound semiconductor" be provided, and that part of the metal layer deposited on the semiconductor body, as well as part of semiconductor body, be dry-chemically removed.

In contrast, Chong describes a method of manufacturing a contact structure and a gate structure having a silicide layer (page 1, paragraph 1). Chong describes, in relation to FIGS. 5-9, that an interdielectric layer 122 is formed on a silicon substrate 120. The interdielectric layer 122 may comprise an oxide film or a nitride film (page 4, paragraph 50). The interdielectric layer 122 is, however, an insulator, not a semiconductor compound. Indeed, nitride-based insulators are commonly used with silicon-based semiconductor devices such as those used by Chong (see, for example, Page 1, paragraph 12). As described, for example, on page 504 of S. M. Sze's "Physics of Semiconductor Devices" (Second Edition, John Wiley & Sons):

> **Among several kinds of MIOS (metal-insulator-SiO_2-Si) memory devices, the MNOS (metal Si_3N_4-SiO_2-Si) device is the most popular. Other MIOS devices use different insulators to replace the silicon nitride film such as aluminum oxide, tantalum oxide, and titanium oxide.**

(A copy of the excerpt from the above-identified Sze reference is attached herewith as Exhibit A for the examiner's convenience.)

Accordingly, Chong does not disclose or suggest at least the feature of "providing a semiconductor body containing a substrate and at least one nitride compound semiconductor disposed on the substrate," as required by applicant's independent claim 1.

Furthermore, Chong additionally describes that a photoresist pattern 124 is applied to the interdielectric material 122, and the interdielectric material 122 is etched to form a contact hole 126 (paragraph 50). After chemically cleaning the contact hole, a first metal layer 128 is deposited on the contact hole (paragraph 67). Subsequently, a silicidation process is applied to the device to cause a silicide layer to form at the bottom of the contact hole 26. The metal layer 128 is then removed, and after applying a further cleaning process to the device, a second metal layer 132 is deposited (paragraph 69-70). However, at no point does Chong describe that any part of the semiconductor body underneath the deposited metal layer is removed, and Chong certainly does not describe that part of the metal layer is removed as well as part of the semiconductor body previously covered by the removed metal parts. Thus, Chong fails to

disclose or suggest at least the feature of "dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal layer," as required by applicant's independent claim 1.

Because Chong does not disclose or suggest at least the features "providing a semiconductor body containing a substrate and at least one nitride compound semiconductor disposed on the substrate" or "dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal layer," applicant's independent claim 1 is patentable over the Chong reference.

Claims 2-25 depend from independent claim 1 and are therefore patentable for at least the same reasons as applicant's independent claim 1.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer. Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Enclosed is a Petition for One Month Extension of Time. The fees in the amount of $120 are being paid concurrently on the Electronic Filing System (EFS) by way of Deposit Account authorization.

Please apply any other required fees to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date: Dec. 5, 2006

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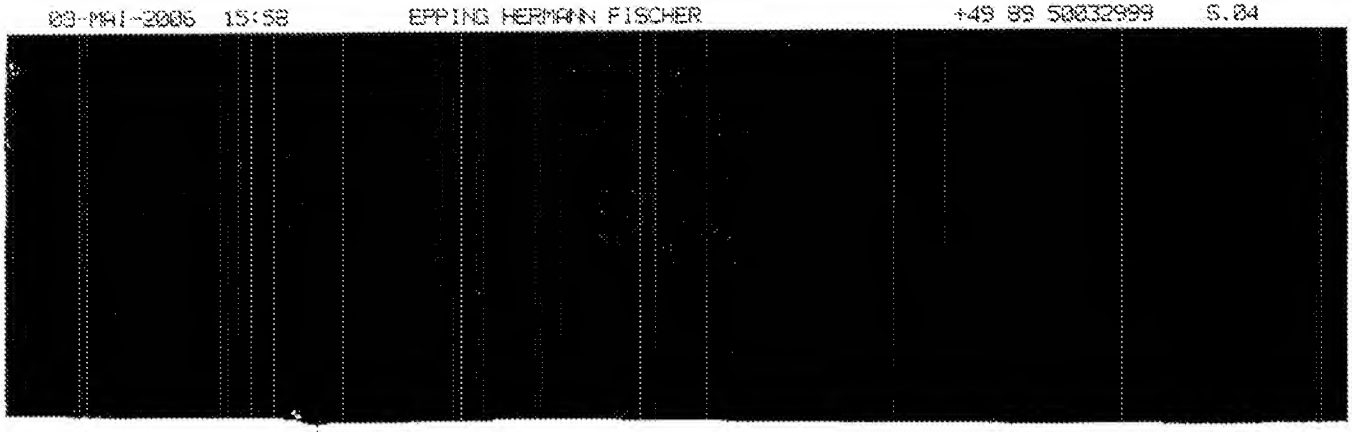
EXHIBIT A



Physics of Semiconductor Devices

SECOND EDITION

S. M. Sze

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Murray Hill, New Jersey

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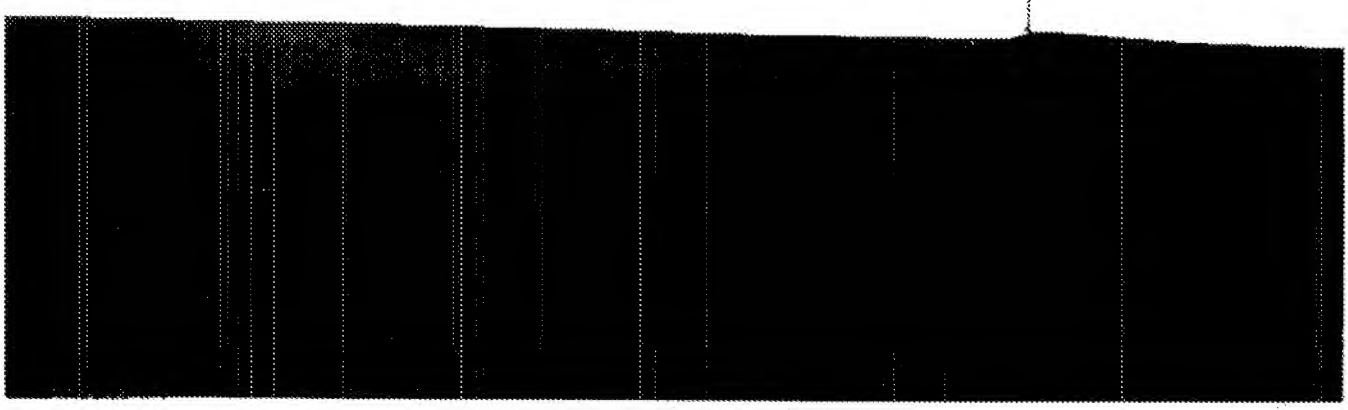

50% of its initial value and is given by

$$t_R \approx \ln 2/[\nu \exp(q\phi_B/kT)] \tag{113}$$

where ν is the dielectric relaxation frequency, and $q\phi_B$ is the barrier height indicated in Fig. 65b. Figure 68 shows typical calculated retention times at 125°C and 170°C with $q\phi_B = 1.7$ eV and compares them with experimental data. The values of retention time for 125°C and 170°C are found to be about 100 years and 8000 h, respectively.

9.6.2 MIOS Device

Among several kinds of MIOS (metal–insulator–SiO_2–Si) memory devices, the MNOS (metal–Si_3N_4–SiO_2–Si) device is the most popular. Other MIOS devices use different insulators to replace the silicon nitride film, such as aluminum oxide, tantalum oxide, and titanium oxide. The MIOS device has been made by using metal ions (e.g., Au) implanted into SiO_2 to alter the conduction properties of the outer oxide to form the interfacial charge storage centers.[76]

Figure 69 shows the basic band diagrams for the writing and erasing operations.[77] The current J_o in the oxide is due to Fowler–Nordheim tunneling, and the current J_N in the silicon nitride is due to Frankel–Poole emission. The equations governing the charging behavior are identical to those described before, Eqs. 105 through 108. However, in a practical device, the traps at the oxide–nitride interface may be distributed across the nitride energy gap and extended from the interface into the bulk nitride. Various models have been considered to achieve better agreement with experimental writing characteristics. A representative result for an MNOS device with 20-Å SiO_2 and 433-Å Si_3N_4 shows that the measured and calculated results are in good agreement (Fig. 70).[78] The figure also shows that the write time to reach a given threshold voltage shift decreases rapidly with increasing V_G. For a given gate voltage the threshold voltage shift tends to saturate at a longer write time, showing the general behavior displayed in Fig. 62.

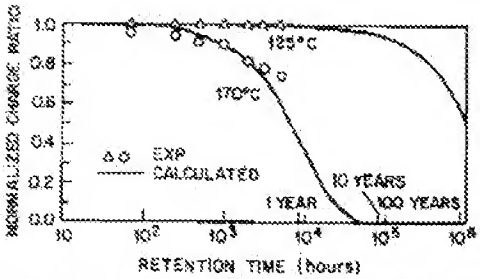

Fig. 68 Normalized charge storage versus time for two ambient temperatures. (After Nishi and Iizuka, Ref. 72.)

Fig. 69 (a) Writing and (b Banichkowsky, Ref. 77.)

To improve MIOS d device (DDC) with ints facial dopant (e.g., tung the insulator–oxide inte or erase operation (Fig device without the inte magnitude faster than conditions of $V_G = 30$ V erasing operation.